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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>26 September 2008</u>.
2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-16</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1-16</u> is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All b) ☐ Some * c) ☐ None of:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed claims 1-16 have been fully considered but they are not

persuasive.

Regarding claims 1-16, the applicant argued that, "…CrystalClear fails to disclose or

suggest a method for communication audio including a number of synchronization markers on a

second signal line, each marker being representative of a timing of one audio information

segment, wherein only a first signal line and the second signal line are used to communicate

audio …" in page 5-8.

In response to applicant's argument, the examiner respectfully disagrees with the

argument above.

CS4205 (refers to as CrystalClear by the applicant) discloses transmitting a number of

synchronization markers (**see FIG. 14, transmitting SYNC pluses; see FIG. 17-20,**

transmitting LRCLK pulses) on a second signal line (**see FIG. 7,14, SYNC/LRCLK line**

(SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24,

paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being representative of a timing

of one of the audio information segments (**see FIG. 14, 17-20; each SYNC/LRCLK pulse**

indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs

4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein <u>only</u> the first signal line (**see FIG. on cover page; see FIG. 7, 14, SD data line**

(OUT, or SDOUT)) and the second signal line are configured to communicate audio (**see FIG.**

7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are used to

communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs

4-5; page 54-58, paragraphs 6.3-9; *note that per FIG. on cover page, FIG. 7, 14, <u>ONLY</u>*

SDATA_OUT signal line and SYNC signal line are sufficient/enough for communicating audio

data; note that RESET # signal line is only utilized for transmission of commands, and it is not

<u>required</u> (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not

required and thus it is not used for communication audio. Only SDATA_OUT signal line and

SYNC signal line are used for communication audio; see page 13 section 2.1;

alternatively, per FIG. on cover page; per FIG. 7, 14, <u>ONLY</u> SDOUT signal line and

LRCLK signal line are used for communicating audio data; *note that SCLK is <u>optional</u> in*

CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for

communication audio. Only SDATA_OUT signal line and LRCLK signal line are used for

communication audio; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see

page 54-56, paragraph 6.4,7).

In view of the above, it is clear that CS4205 clearly discloses the broadly claimed

invention.

Regarding claims 1-16, the applicant argued that, "…CrystalClears requires at least

three wires for proper audio communication, not only two as recited in applicant's claims…the

following wires are necessary...(1) BIT CLK...(2) SYNC...(3) SDATA OUT/SDATA IN..." in

pages 5-8.

In response to applicant argument, it is noted that applicant <u>erroneous</u> argument is

based on <u>incorrectly</u> counting every possible connections of CS4205 (e.g. (1) BIT CLK...(2)

SYNC...(3) SDATA OUT/SDATA IN), and where the claim invention recites "<u>transmitting</u>....on

a first signal line", "transmitting...on a second signal line", and the claimed invention shown in

FIG. 1-2, transmitter transmitting first signal line and second signal line. Thus, examiner is

asserting the applicant claimed invention in light of the specification, the first signal line as

transmitting SD data line (OUT, or SDOUT) and the second signal line as transmitting

SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the

claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

 In response to applicant argument, applicant erroneously **assuming** and arguing the

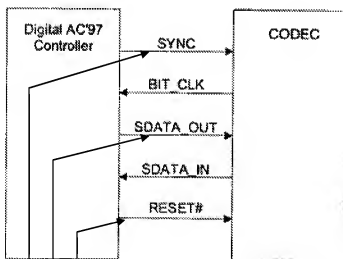incorrect facts in CS4205. The following detailed examiner assertions.

Figure 7. AC-link Connections

  RESET is optional – not use for transmitting audio- only used for
transmitting of commands (see CS4205 page 13, section 2.1)

 SDATA_OUT is a **FIRST SIGNAL LINE** that transmit audio
information segments

 SYNC is a SECOND SIGNAL LINE that transmits a number of
synchronization markers

In view of the CS4205 FIG. above, it is clear that ONLY a first signal line and a second

signal line are used for <u>transmitting</u> communication audio information segments. Also, one

skilled in the ordinary would clearly see that RESET signal line is only for commands, and it is

not used in communication audio.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
> sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claim 1-4, 6, 8-14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by

CS4205 (CyrstalClear Audio Codec '97 product information document).

Regarding Claim 1, CS4205 Reference discloses a method for communicating audio

(see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing

coding and decoding steps/methods), comprising:

transmitting audio information segments on a first signal line (see FIG. on cover page;

see FIG. 7, 14, 16-20, 35, SD data line (OUT, or SDOUT) transmits each audio frame

segment/portion/frame), each segment (see FIG. 14, 17-20, each audio frame) including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes

(see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1, 4.1.1-4.1.5; slots 0-2

contains audio format/arrangement/layout indication/signals (e.g. tags, command address,

command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes))

and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one

or more of the format modes (see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs

4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that

corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

transmitting a number of synchronization markers (see FIG. 14, transmitting SYNC

pluses; see FIG. 17-20, transmitting LRCLK pulses) on a second signal line (see FIG. 7,14,

SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph

2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being

representative of a timing of one of the audio information segments (see FIG. 14, 17-20; each

SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page

19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein only the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line

(OUT, or SDOUT) and the second signal line are configured to communicate audio (see FIG.

7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are used to

communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5;

page 54-58, paragraphs 6.3-9; *note that per FIG. on cover page, FIG. 7, 14, ONLY*

SDATA_OUT signal line and SYNC signal line are sufficient/enough for communicating audio

data; note that RESET # signal line is only utilized for transmission of commands, and it is not

required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not

required and thus it is not used for communication audio. Only SDATA_OUT signal line and

SYNC signal line are used for communication audio; see page 13 section 2.1;

<u>alternatively</u>, per FIG. on cover page; per FIG. 7, 14, <u>ONLY</u> SDOUT signal line and

LRCLK signal line are used for communicating audio data; *note that SCLK is <u>optional</u> in*

CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for

communication audio. Only SDATA_OUT signal line and LRCLK signal line are used for

communication audio; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see

page 54-56, paragraph 6.4,7).

Regarding Claim 2, CS4205 Reference discloses the audio comprises a serial bit stream

(see page 13, paragraph 2.1; audio stream is a serial bit stream).

Regarding Claim 3, CS4205 Reference discloses the information segments are

unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5,

4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated

in CS4205).

Regarding Claim 4, CS4205 Reference discloses the information segments are

representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-

3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more

audio channels/slots).

Regarding Claim 6, CS4205 Reference discloses wherein the format modes include at

least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1,

4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data,

or AC/Analog/digital/host processing/multi-channel mode)).

Regarding Claim 8, CS4205 Reference discloses the format modes are dynamic (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame, thus the audio format/arrangement/layout are dynamic).

Regarding Claim 9, CS4205 Reference discloses the format modes are configured to vary from one information segment to another information segment (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame).

Regarding Claim 10, CS4205 Reference discloses the synchronization marker include sync pulses (see FIG. 14, 17-20; each SYNC/LRCLK pulse; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 11, CS4205 Reference discloses each sync pulse represents a start of one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 12, CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

transmitting audio information segments on a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line (IN, or SDI1-3) receives each audio frame segment/portion/frame), each segment (see FIG. 14, 17-20, each audio frame) including

receiving audio information segments on a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line (IN&OUT, or SDOUT & SDI1-3), each segment including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

receiving a number of synchronization markers (see FIG. 14, receiving SYNC pluses; see FIG. 17-20, transmitting LRCLK pulses) on a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being represented of a timing of one of the audio segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein <u>only</u> the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line

(OUT, or SDOUT) and the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC &

BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-

5; page 54-58, paragraphs 6.3-9) are used to communicate audio (see FIG. 7,14, and

SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are arranged/configured to

communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5;

page 54-58, paragraphs 6.3-9); *note that per FIG. on cover page, FIG. 7, 14, <u>ONLY</u>*

SDATA_OUT signal line and SYNC signal line are sufficient/enough for communicating audio

data; note that RESET # signal line is only utilized for transmission of commands, and it is not

<u>required</u> (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not

required and thus it is not used for communication audio. Only SDATA_OUT signal line and

SYNC signal line are used for communication audio; see page 13 section 2.1;

<u>Alternatively</u>, per FIG. on cover page; per FIG. 7, 14, <u>ONLY</u> SDOUT signal line and

LRCLK signal line are used for communicating audio data; *note that SCLK is <u>optional</u> in*

CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for

communication audio. Only SDATA_OUT signal line and LRCLK signal line are used for

communication audio; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see

page 54-56, paragraph 6.4,7).

Regarding Claim 13, CS4205 Reference discloses the information segments are

unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5,

4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated

in CS4205).

Regarding Claim 14, CS4205 Reference discloses the information segments are

representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-

3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more

audio channels/slots).

Regarding Claim 16, CS4205 Reference discloses each sync pulse represents a start of

one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates

the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-

4.1.5; see page 54-56, paragraph 6.4,7).

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.   Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205

in view of Wolf (US007088398B1).

Regarding Claim 5, CS4205 Reference discloses wherein the format portion comprises a

total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21,

paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags,

command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-

channel modes in slots 0-2 which contain total 56 bit data word).

CS4205 Reference does not explicitly disclose 32 bits. However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the system of CS4205, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

Regarding Claim 15, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

CS4205 Reference does not explicitly disclose 32 bits.

However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the system of CS4205, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

6.   Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 in view of Wakazu (US006006287A).

Regarding Claim 7, CS4205 Reference discloses wherein the format modes include at least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode)), and transmission of one or more one or more of the transmitted audio segments/frames to an intended recipient (see FIG. 7, controller, see FIG. 16, Stereo DACs) as set forth above in claim 1.

CS4205 Reference does not explicitly disclose audio stream ID includes an indication of an intended recipient.

However, Wakazu teaches the audio stream ID (see FIG. 4, Audio stream ID 2; see FIG. 6, Audio stream IDs A1-A5) includes an indication of an intended recipient of one or more of the transmitted audio segments (see FIG. 2, audio stream ID indicates/identifies the receiver processor 211 or processor 210; see col. 5, line 10 to col. 6, line 60).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide audio stream ID includes an indication of an intended recipient, as taught by Wakazu in the system of CS4205, so that it can separate/detect the received data stream according to the stream ID; see Wakazu col. 2, line 10-15, 40-49.

Conclusion

7.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

       If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

       Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

                                             Ian N. Moore

Primary Examiner
Art Unit 2416

/Ian N. Moore/
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